interface between the metal Ge compound layer and the Ge layer can be improved. Accordingly, it is possible to improve device characteristics of a semiconductor device including a metal Ge compound layer formed on a semiconductor layer including Ge as a main component.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor layer including Ge; and

a metal Ge compound region provided in a surface portion of the semiconductor layer,

wherein Sn is included in an interface portion between the semiconductor layer and the metal Ge compound region,

a lattice plane of the semiconductor layer matches with a lattice plane of the metal Ge compound region, and

the lattice plane of the semiconductor layer is a (01-1) plane and the lattice plane of the metal Ge compound region is a (121) plane.

2. The device of claim **1**, wherein the surface of the semiconductor layer is a (100) plane.

3. The device of claim **1**, wherein a concentration of Sn in the interface portion is higher than a concentration of Sn in a portion of the metal Ge compound region except the interface portion.

4. The device of claim **1**, wherein the metal Ge compound region includes at least one metal selected from the group consisting of Ni, Fe, Co, Pd, Pt and Cu.

5. The device of claim **1**, wherein the surface portion of the semiconductor layer includes an impurity different from a semiconductor material of the semiconductor layer.

6. A semiconductor device comprising:

a first conductivity type semiconductor layer including Ge;

first and second metal Ge compound regions, which are provided in a surface portion of the first conductivity type semiconductor layer and spaced apart from each other; and

a gate electrode provided on a gate insulating film on a region interposed between the first and second metal Ge compound regions in the first conductivity type semiconductor layer,

wherein

Sn is included in interface portions between the first conductivity type semiconductor layer and each of the first and second metal Ge compound regions,

a lattice plane of the first conductivity type semiconductor layer matches with a lattice plane of each of the first and second metal Ge compound regions, and

the lattice plane of the first conductivity type semiconductor layer is a (01-1) plane and the lattice plane of each of the first and second metal Ge compound regions is a (121) plane.

7. The device of claim **6**, wherein the surface of the first conductivity type semiconductor layer is a (100) plane.

8. The device of claim **6**, wherein concentrations of Sn in the interface portions are higher than concentrations of Sn in portions of the first and second metal Ge compound regions except the interface portions.

9. The device of claim **6**, wherein the first and second metal Ge compound regions include at least one metal selected from the group consisting of Ni, Fe, Co, Pd, Pt and Cu.

10. The device of claim **6**, wherein the surface portion of the first conductivity type semiconductor layer includes an impurity different from a semiconductor material of the first conductivity type semiconductor layer.

11. The device of claim **6**, wherein the first conductivity type semiconductor layer is one of a p-type semiconductor layer and an n-type semiconductor layer.

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